

$$\begin{aligned} \frac{\partial}{\partial t} \left( \frac{1}{2} \rho \mathbf{u} \cdot \mathbf{u} \right) + \nabla \cdot \left( \frac{1}{2} \rho \mathbf{u} \otimes \mathbf{u} \right) &= \rho \mathbf{u} \cdot \nabla \mathbf{u} + \nabla \cdot \left( \frac{1}{2} \rho \mathbf{u} \otimes \mathbf{u} \right) \\ &= \rho \mathbf{u} \cdot \nabla \mathbf{u} + \nabla \cdot \left( \frac{1}{2} \rho \mathbf{u} \otimes \mathbf{u} \right) \\ &= \rho \mathbf{u} \cdot \nabla \mathbf{u} + \nabla \cdot \left( \frac{1}{2} \rho \mathbf{u} \otimes \mathbf{u} \right) \end{aligned}$$

## Abstract of Disclosure

A memory device and a fabrication method thereof, wherein the memory device includes a gate oxide layer disposed on a surface of the substrate and a gate disposed on a portion of the gate oxide layer. A buried drain line is located in the substrate beside both sides of the gate and a spacer is disposed beside the sidewalls of the gate. A deep doped region is located in the substrate below a portion of the buried drain line, wherein the buried drain line and the deep doped region together serve as a word line for the memory device. An insulation layer is disposed above the bit line and a word line is disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

## Figures